Listing of Claims

1. (Original) A system, comprising:

a clock generator to generate a number of clock signals having equally spaced phases determined by a predetermined fraction of a data rate frequency of a data stream; and

a sampling unit to sample the data stream based on the clock signals.

2. (Original) The system of claim 1, wherein each of the clock signals has a frequency determined by the predetermined fraction of the data rate frequency of the data stream.

3. (Original) The system of claim 2, wherein the predetermined fraction is N, the equal phase spacing of the clock signals is 360°/N, and the frequency of each clock signal is equal to 1/N of the data rate frequency of the data stream.

4. (Original) The system of claim 1, wherein the sampling unit includes a number of samplers which sample the data stream based on different combinations of the clock signals.

5. (Original) The system of claim 4, wherein each sampler samples the data stream based on a different pair of the clock signals.

6. (Original) The system of claim 4, wherein the number of samplers equals to the number of clock signal phases generated by the clock generator.

7. (Original) The system of claim 4, wherein the number of samplers and the number of clock signal phases generated by the clock generator are different.

8. (Original) The system of claim 4, wherein each of the samplers sample the data stream based on a different pair of clock signals having consecutive phases.

9. (Original) The system of claim 1, where the equal spacing of the clock signal phases corresponds to a symbol duration of the data stream.

10. (Original) The system of claim 1, further comprising:

a converter to convert an optical data stream into an electrical data stream,

wherein the sampling unit samples the electrical data stream based on the clock signals.

11. (Original) The system of claim 10, wherein the data rate frequency is a data rate frequency of the optical data stream sampled by the sampling unit.

12. (Original) A data sampling method, comprising:

generating a number of clock signals having equally spaced phases, each of said phases determined by a predetermined fraction of a data rate frequency of a data stream; and

sampling the data stream based on the clock signals.

13. (Original) The method of claim 12, wherein each of the clock signals has a frequency determined by the predetermined fraction of the data rate frequency of the data stream.

14. (Original) The method of claim 13, wherein the predetermined fraction is N, the equal phase spacing of the clock signals is 360E/N, and the frequency of each clock signal is equal to 1/N of the data rate frequency of the data stream.

15. (Original) The method of claim 12, wherein sampling the data stream includes: sampling the data stream based on different combinations of the clock signals.

16. (Original) The method of claim 12, wherein sampling the data stream includes: sampling the data stream based on a different pair of the clock signals.

17. (Original) The method of claim 16, wherein the different pair includes clock signals having consecutive phases.

18. (Original) The method of claim 12, wherein sampling the data stream includes: sampling the data stream using a number of samplers equal to the number of generated clock signal phases.

19. (Original) The method of claim 12, wherein sampling the data stream includes: sampling the data stream using a number of samplers different from the number of generated clock signal phases.

20. (Previously Presented) The method of claim 12, where the equal spacing of the clock signal phases corresponds to a symbol duration of the data stream.

21. (Original) The method of claim 12, further comprising:

converting an optical data stream into an electrical data stream, wherein sampling the data stream includes sampling the electrical data stream based on the clock signals.

22. (Original) The method of claim 21, wherein the data rate frequency is a data rate frequency of the optical data stream.

23. (Previously Presented) A data sampler, comprising:

a sampling stage to sample data based on clock signals having different phases; and

a buffer to stored the sampled data, wherein the difference between the phases of the clock signals at least substantially equals a symbol duration of the data.

24. (Canceled)

25. (Original) The data sampler of claim 23, wherein the buffer includes a static latch.

26. (Previously Presented) A method, comprising:

sampling a data stream based on clock signals having different phases; and

storing the sampled data in a storage circuit, wherein the difference between the phases of the clock signals at least substantially equals a symbol duration of the data.

27. (Canceled)

28. (Original) The method of claim 26, wherein the storage circuit includes a static latch.

29. (Original) A system, comprising:

a processor; and

a sampling unit including:

(a) a clock generator to generate a number of clock signals having equally spaced phases determined by a predetermined fraction of a data rate frequency of a data stream; and

(b) a sampling unit to sample the data stream based on the clock signals.

30. (Original) The system of claim 29, where the equal spacing of the clock signal phases corresponds to a symbol duration of the data stream.

31. (Previously Presented) The system of claim 4, wherein the samplers sample the data stream based on sampling signals that are generated by different pairs of the clock signals.

32. (Previously Presented) The system of claim 31, wherein consecutive pairs of clock signals share a common clock signal.

33. (Previously Presented) The system of claim 31, wherein the clock signals in each pair have consecutive phases.

34. (Previously Presented) The system of claim 33, wherein the sampling signals having non-overlapping duty cycles.

35. (Previously Presented) The system of claim 33, wherein the sampling signals have overlapping duty cycles.

36. (Previously Presented) The system of claim 33, wherein the clock signals in each pair define different edges of corresponding ones of the sampling signals.

37. (Previously Presented) The system of claim 33, wherein the sampling signals have duty cycles which are substantially different from 50%.

38. (New) The system of claim 1, wherein the sampling unit includes a plurality of samplers which sample the data stream based on different pairs of the clock signals that have consecutive overlapping phases.